AMENDMENTS TO THE DRAWINGS:

Please add new Fig. 1C. Support for Fig. 1C can be found, e.g., on pages 9 and 13 of the specification currently on file (the translation of the German-language PCT application).

REMARKS

Claims 1 to 29 are pending in the application, of which claims 1 and 26 are independent. Favorable reconsideration and further examination are respectfully requested.

Initially, the drawings were objected to for allegedly not showing a stripline filter and casting compound. As shown above, Applicant has added new Fig. 1C, which includes those features. Withdrawal of the objection to the drawings is therefore respectfully requested.

Next, the claims were objected to under the first paragraph of 35 U.S.C. §112 for allegedly failing to shown that the integrated impedance converter is configured to perform impedance conversion by at least a factor of two. Without conceding the propriety of the rejection, and solely to advance prosecution, Applicant has amended independent claims 1 and 26 to recite that the integrated impedance converter is configured to perform impedance conversion between different standard impedance levels. Support for this amendment can be found, e.g., on the first paragraph of page 5 of the specification. In view of this amendment, withdrawal of the §112 rejection is respectfully requested.

Turning to the art rejections, claims 1, 2, 3, 10, 16, 22, 23, and 25 to 27 were rejected over U.S. Patent No. 5,818,699 (Fukuoka); claim 4 was rejected over Fukuoka in view of U.S. Patent No. 6,970,362 (Chakravorty); claims 5, 11, 12, 13, 15, 19, 20, 21 and 28 were rejected over Fukuoka in view of U.S. Patent No. 6,628,178 (Uchikoba); claim 6 was rejected over Fukuoka in view of U.S. Patent No. 6,673,697 (Ma); claim 7 was rejected over Fukuoka in view of U.S. Patent No. 6,713,860 (Li); claim 8 was rejected over Fukuoka in view of U.S. Patent No. 6,955,948 (Asahi); claim 9 was rejected over Fukuoka in view of U.S. Patent No. 6,388,207 (Figueroa); claim 14 was rejected over Fukuoka and Uchikoba in view of U.S. Patent No.

6,060,954 (Liu); claims 17 and 18 were rejected over Fukuoka in view of the Harper article; and claim 29 was rejected over Fukuoka in view of U.S. Patent No. 6,356,453 (Juskey). Although Applicant has amended the independent claims, that amendment was made to address the §112 rejection. Accordingly, this should be viewed as a traversal of the art rejection.

Independent claims 1 and 26 each include a multi-layer substrate having an upper side and under side, where the multi-layer substrate comprises at least one integrated impedance converter, and where the at least one integrated impedance converter is configured to perform impedance conversion between different standard impedance levels. The applied art is not understood to disclose or to suggest at least this feature of the claims.

In this regard, the Office Action equates element 202b of Fukuoka, Fig. 8, to the integrated impedance converter of the claims. As explained in column 16 of Fukuoka, element 202b is a chip resistor, which is "face-up bonded on the first surface of a substrate 101" (lines 55 to 58). Thus, chip resistor 202b in Fukuoka is external to its substrate 101. By contrast, in claims 1 and 26, the multi-layer substrate comprises an integrated impedance converter, meaning that the impedance converter at least partly integrated into the multi-layer substrate (see, e.g., element IW in Fig. 1A of the specification). As explained, e.g., on page 5 of the application, an integrated construction has advantages over non-integrated constructions, such as that of Fukuoka, both in terms of space saving and manufacturing.

The remaining art has not been cited for, nor does it show, a multi-layer substrate comprising at least one integrated impedance converter, where the at least one integrated impedance converter is configured to perform impedance conversion between different standard impedance levels. Accordingly, claims 1 and 26 are believed to be patentable.

Each of the dependent claims is also believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim and, as such, has not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicant respectfully submits that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Please charge any additional fees, not already covered by check, or credit any overpayment, to deposit account 06-1050, referencing Attorney Docket No. 14219-075US1.

Finally, Applicant is submitting herewith a Supplemental Declaration to correct a minor informality in the Declaration currently on file. In the Declaration currently on file, the U.S. serial number and filing date were added post-signing (when that information was added to the Assignment document).

Applicant's attorney can be reached at the address shown above. Telephone calls regarding this application should be directed to 617-521-7896.

Respectfully submitted,

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ELECTRONIC COMPONENT

Technical Field

The ~~invention~~ patent application relates to an electronic component or module having a chip component, especially a filter, and a multi-layer substrate, as well as a process for assembly of the chip component on the multi-layer substrate.

Background

An electronic module is a highly-integrated component, which comprises one or more circuits monolithically integrated into a multi-layer substrate and fulfills various functions, in the terminal device of a mobile communication system, for example.

An electronic module can, for example, perform the function of an antenna circuit, a duplexer, a diplexer, a coupler, etc.

In addition to the integrated circuits, a module can contain one or more chip components as well as discrete circuit elements or components, which are disposed with the integrated circuit elements on the upper side of the multi-layer substrate.

It is frequently necessary to obtain a symmetrical signal at the output end of a chip component. To this end, either a balun can be integrated directly into the structure of the chip component, or a chip component having asymmetrical inputs and outputs and a

downstream balun comprising discrete individual elements can be used. Such a balun can be executed as a compact, individual component.

To achieve a higher degree of integration, it is possible to arrange the chip component having upstream and downstream functional units on a shared dielectric substrate. In this manner, front end modules for time-duplexed systems such as GSM900/1800/1900 can be obtained, for example, when SAW filters (SAW = surface acoustic wave) are disposed on a multi-layer ceramic substrate together with the circuit elements of an antenna circuit. In this regard, the circuit elements of the antenna circuit can be partially integrated in the multi-layer substrate.

To achieve optimal signal transmission in the range of the pass band, it is necessary that the output impedance of a chip component be perfectly adjusted to the input impedance of the subsequent stage and/or that the input impedance of a chip component be perfectly adjusted to the output impedance of the upstream stage. Thus, to allow for their adjustment to their circuit environment, the chip components require an electric adjustment network. Such a network can comprise inductances, ~~capacities~~ capacitances and delay lines, and its principal purpose is to adjust the impedance of a component to the external environment. It is known that an adjustment network can be executed, wherein the chip component, together with the discrete individual components, is soldered to a printed circuit board.

It is known that an SAW component having a multi-layer carrier substrate (made of ceramics, for example), which comprises integrated adjustment elements, can be attached and electrically connected by means of a flip-chip array or by means of wire bonding. See, for example, document US 5,459,368. In addition to one or more SAW chips, additional passive or active, discrete circuit elements can be disposed on the upper side of the carrier substrate. However, the production of such components is complex and expensive, because SAW chips and/or so-called circuit elements are electrically connected with the carrier substrate by means of various connection methods.

If, for example, a chip component is connected in a reception branch in front of one or between two LNAs (low noise amplifier), the terminal impedance values that occur usually range between 50 and 200 Ohm. If the impedances of the upstage and downstage stages are known, it is essentially possible to execute the chip component in such a way that its input and/or output impedances correspond to the required values. In previously known chip components, the entire component had to be completely redeveloped for each application with the predetermined input and/or output impedance (e.g., 25, 50, 200 Ohm).

However, the range of available terminal impedances for components is often limited (especially in the case of SAW components).

External impedance converters equipped with discrete individual components can also be used. In the latter case, this results in an increase in space requirements. In addition, the reliability of the overall design suffers as a result of the required connection points.

Summary

~~The goal of the present invention is to provide a highly integrated component, which comprises a chip component, a multi-layer substrate electrically connected to it, and an impedance converter.~~

~~This goal is achieved, according to the invention, by means of a component with the features of Claim 1. Advantageous further developments of the invention are found in the additional claims.~~

~~The invention provides~~ This application describes an electronic component, which comprises a) a multi-layer substrate, b) at least one chip component having external contacts, and c) at least one impedance converter (monolithically) integrated into the multi-layer substrate. At least one chip component is disposed on the upper side of the multi-layer substrate and is electrically connected with the impedance converter.

A chip component is defined as a "naked" chip having electronic structures or an embedded chip having such structures.

An impedance converter is defined~~, within the meaning of the invention,~~ herein as an electronic circuit which fulfills an impedance transformation, that is, which changes actual impedance values characteristic for a chip component or for all chip components of the same type to a predetermined reference value. At issue are not just significant differences between actual and reference impedance values (e.g., a multiplication of impedance from 50 to 200 Ohm), but also relatively small differences of less than 100%, but at least 5% between actual and reference impedance values (e.g., a change in impedance from 46 to 50 Ohm). In contrast, in the present ~~applicable~~ application, an adjustment or impedance adjustment is defined as a desired change in impedance of no more than 5%, that is, offsetting a production-related defective adjustment.

An advantage of the component ~~according to the invention~~ described herein is that the impedance converter required for an impedance transformation, in contrast to known solutions, is not disposed on a printed circuit board, but instead is integrated in the multi-layer substrate, wherein the same multi-layer substrate bears a chip component. The total space requirement is especially small in this arrangement, because the integration takes place in a vertical direction. A compact unit encompassing the multi-layer substrate having the integrated impedance converter guaranties the required impedance transformation and can be pre-manufactured by standard means. This unit can easily and quickly transform the characteristic actual impedance of chip components manufactured by standard means to a different required output impedance value. This eliminates the

need for new development of the entire chip component, as well as the associated costs and time loss.

In and advantageous embodiment, the component ~~according to the invention~~ described herein can also comprise one or more discrete passive or active circuit elements. In this case, ~~said~~ the circuit elements are disposed on the upper side of the multi-layer substrate.

The discrete passive or active circuit elements can form at least a part of the following circuits: a high-frequent circuit, an adjustment circuit, an antenna circuit, a diode circuit, a transistor circuit, a high-pass filter, a low-pass filter, a band-pass filter, a band elimination filter, a power amplifier, a pre-amplifier, an LNA, a diplexer, a duplexer, a coupler, a directional coupler, a memory element, a balun, a mixer or an oscillator.

The integrated circuit elements can, for example, establish electric connections between an antenna and the band pass filters in the reception or transmission path of a component ~~according to the invention~~ constructed as a diplexer and, furthermore, improve upon electric filter characteristics in general and, in particular, insulate the reception and transmission ports from one another.

The integrated circuit elements ~~are preferably~~ may be disposed in a multi-layer ceramic material, such as LTTC ceramics (= low temperature cofired ceramics). LTTC

material allows for a high integration density of network elements. Alternatively, a multi-layer substrate can comprise layers of HTCC (= high temperature cofired ceramics), silicon and other semiconductors (e.g., GaAs, SiGe, silicon oxide, other oxides) or organic materials (e.g., laminates, plastic).

The multi-layer substrate has both internal electric terminals on the upper side, for contacting the chip component, of which there is generally one, and, if applicable, the discrete circuit element, of which there is generally one, as well as external electrodes on the lower side, to establish an electric connection between the component and an external printed circuit board, such as that of a terminal device.

In the following, the ~~invention~~ component is explained in greater detail on the basis of exemplary embodiments and the corresponding figures. The figures are provided for explanatory purposes only and are not true to scale. Identical elements are identified with the same reference numbers.

Description Of The Drawings

Figure 1, comprised of Figs. 1A, 1B and 1C, shows the basic structure of a component ~~according to the invention~~ in schematic cross-section (Figure 1A and 1C) and ~~as well as a~~ top view ~~of a component according to the invention~~ (Figure 1B).

Figure 2 shows an ~~advantageous~~ embodiment of a component ~~according to the invention,~~ having an integrated coil and an integrated capacitor.

Detailed Description

The component shown in Figure 1A is constructed as a multi-layer component having a multi-layer substrate MS, at least one chip component CB being disposed on the lower side of the multi-layer substrate. The chip component can be either a "naked" chip having electronic structures or a chip having a housing GE. It is possible that the chip component also contains a multi-layer substrate having integrated passive or active circuit elements.

~~Within the meaning of the invention~~ In the context of this application, a passive or active circuit element is defined, in particular, as an inductance, a capacity, a delay line, a resistor, a diode or a transistor. In addition, a discrete passive or active circuit element can comprise any combination or the above-mentioned passive or active components in a compact component.

The chip component formed as a "naked" chip can be attached to the multi-layer substrate or electrically connected with the circuit elements integrated therein by means of bonding wire or flip-chip technology. The external contacts AE of a chip component can also be SMD contacts (SMD = surface mounted design/device).

The chip component can comprise one or more resonators operating with surface acoustic waves and/or bulk acoustic waves, known as SAW and/or BAW resonators or

FBAR (SAW = surface acoustic wave, BAW = bulk acoustic wave, FBAR = thin film bulk acoustic wave resonator).

The chip component can be a chip having one or more filter circuits (filter chip), for example, SAW components such as SAW filters, BAW filters, LC chip filters, stripline filters (see, e.g., Fig. 1C) or microwave ceramic filters.

The at least one chip component CB is electrically connected with an impedance converter IW integrated in the multi-layer substrate MS. The multi-layer substrate can also contain at least one additional integrated circuit element. Another possibility ~~consists in~~ includes a plurality of ~~said~~ integrated circuit elements forming a part of the following circuits: a high-frequency circuit, an adjustment circuit, an antenna circuit, a diode circuit, a transistor circuit, a high-pass filter, a low-pass filter, a band-pass filter, a band elimination filter, a power amplifier, an LNA, a pre-amplifier, a diplexer, a duplexer, a coupler, a directional coupler, a memory element, a balun, a mixer or an oscillator.

In this regard, the integrated circuit elements ~~are preferably~~ may be formed, in a manner known in the art, as strip conductors or randomly shaped metal surfaces in, on or between the individual layers of the multi-layer substrate (substrate layers), as vertical feedthroughs DK in the multi-layer substrate, or as a combination of these elements. It is possible that a part of the integrated circuit elements - that is, at a part of an adjustment circuit - is formed on the upper side of the multi-layer substrate for later fine-tuning by

means, for example, of the partial removal of the existing strip conductors or by means of the subsequent addition of discrete circuit elements.

A plurality of the chip components disposed on the upper side of the multi-layer substrate can either have a shared impedance converter and/or a shared adjustment circuit or individual impedance converters and/or individual adjustment circuits.

The multi-layer substrate can contain, for example, layers of ceramic, silicon, oxides (e.g., silicon dioxide) or organic materials.

The external electrodes AE1 of the component ~~according to the invention~~ on the lower side of the multi-layer substrate can constitute SMD contacts.

In addition, at least one discrete passive or active circuit element SE is visible on the lower side of the multi-layer substrate in Figure 1A.

Figure 1B shows a top view of a component ~~according to the invention~~ having two chip components CB1 and CB2 and three discrete circuit elements SE1, SE2 and SE3. The discrete circuit elements contain electrodes EL.

~~A~~ The component ~~according to the invention~~ described herein can have one or more signal inputs and/or outputs, wherein each individual signal input and/or signal

output can be symmetrical or asymmetrical. In the case of symmetrical signal inputs and/or signal outputs, a coil and/or a capacitor between the two symmetrical signal lines may be added as additional basic elements.

In a further advantageous embodiment, a sheathed chip component (for example, a SAW chip, referred to in the following as a SAW filter) is disposed on the surface of a multi-layer substrate (for example, an LTCC of HTCC multi-layer ceramic) having an integrated impedance converter. The impedance converter comprises a series inductance, which is connected to the output of the chip component and/or of the SAW filter and connects it with an external electrode on the lower side of the multi-layer substrate. The external electrode is used to solder the complete component to a printed circuit board. The series inductance is achieved by means of structured strip conductors and/or strip conductor segments LA (as indicated in Figure 2), which are disposed below an electric contact (external electrode of the chip component) suitable for soldering the chip component and/or the SAW filter. The strip conductors are separated from one another by dielectric layers of the multi-layer substrate. In this regard, the strip conductors of the individual conductor levels LE indicated to the left in Figure 2 are connected with one another by means of feedthroughs DK1, so that a continuous coil winding results. In this regard, the chip component and/or the SAW filter ~~is preferably~~ may be disposed in such a way that its output electrode is located directly above the external electrode AE1 on the lower side of the multi-layer substrate. In a chip component operating with acoustic waves, the coil winding ~~is preferably~~ may be disposed underneath the chip component in

such a way that it is not located directly below active filter structures of the chip component, otherwise, unwanted electromagnetic couplings would arise, which impair the electric component characteristics. For this reason, other integrated components of the impedance converter, especially in the uppermost layers of the multi-layer substrate, should be disposed, if possible, below the external contacts of the chip component and not below active structures of the chip component.

A ground shield GS located in the lowermost layer of the multi-layer substrate forms a capacity for the windings of the series inductance disposed above it, which constitutes an integrated coil. As a result, mirror currents are induced, which reduce the inductance value of the integrated coil. Larger inductance values can be achieved by maintaining a relatively large distance (e.g., at least 150 μm with strip conductors that are 100 μm wide) between the coil and the lower shield layer.

In the embodiment of the component ~~according to the invention~~ shown in Figure 2, its output impedance can be transformed from a higher to a lower impedance value. The underlying circuit comprises a series inductance (coil) connected to the output of the chip component and a capacitor to ground. The capacitor to ground is constructed as follows: A line is branched off at the terminal of the coil on the side of the chip component, this line being, for the most part, formed with feedthroughs DK1, so that this line progresses vertically downward in the multi-layer substrate and, at its end, contacts a metal plate MP, which is separated from the ground shield layer GS by only one dielectric layer, for

example, forming a capacitor with the latter. The element identified by the reference symbol K is used here for explanatory purposes only.

In another ~~advantageous~~ embodiment ~~of the invention~~, the chip component has a symmetrical output. The two contacts of the symmetrical output ~~are preferably~~ may be disposed directly and/or symmetrically above the corresponding external electrode on the lower side of the multi-layer substrate. The integrated coils, e.g., series coils, which are part of the integrated impedance converter, can be symmetrically or offset symmetrically coiled.

It is possible that a capacitor executed in the multi-layer substrate is connected between the two contacts of the symmetrical output of the chip component. In this regard, ~~said~~ the contacts are connected with parallel metal plates disposed in lower layers by means of feedthroughs.

In another embodiment, an integrated impedance converter can contain a coil connected to ground. In this regard, one end of the coil is connected, on the one hand, to a ground shield surface, which, for example, is disposed in one of the lower layers of the multi-layer substrate, and, on the other hand, to an external electrode of the chip component by means of a feedthrough.

It is possible that the at least one chip component CB disposed on the upper side of the multi-layer substrate is mechanically stabilized with one or more circuit elements SE by means of a casting compound (CC in Fig. 1C), such as Globtop, e.g., with casting resin in an epoxy base.

Claims

1. Electronic component containing:

- a multi-layer substrate (MS),

- at least one chip component (CB) having external contacts (AE), wherein the at least one chip component (CB) is disposed on the upper side of the multi-layer substrate (MS), characterized in that

at least one integrated impedance converter (IW) is disposed in the multi-layer substrate (MS), wherein the at least one chip component (CB) is electrically connected with the at least one integrated impedance converter (IW).

2. Component according to Claim 1,

in which the external contacts (AE) of the at least one chip component (CB) constitute SMD contacts.

3. Component according to Claim 1 or 2,

in which the multi-layer substrate (MS) comprises, in addition to the impedance converter, at least one additional integrated passive or active circuit element.

4. Component according to at least one of Claims 1 to 3,

in which the at least one chip component (CB) comprises at least one filter circuit.

5. Component according to at least one of Claims 1 to 4,

in which the at least one chip component (CB) comprises at least one resonator operating with surface acoustic waves.

6. Component according to at least one of Claims 1 to 5,

in which the at least one chip component (CB) comprises a resonator operating with bulk acoustic waves.

7. Component according to at least one of Claims 1 to 6,

in which the at least one chip component (CB) is a microwave ceramic filter.

8. Component according to at least one of Claims 1 to 7,

in which the at least one chip component (CB) is an LC chip filter.

9. Component according to at least one of Claims 1 to 8,

in which the at least one chip component (CB) is a stripline filter.

10. Component according to at least one of Claims 1 to 9,

in which at least one discrete passive or active circuit element (SE) is disposed on the upper side of the multi-layer substrate (MS).

11. Component according to at least one of Claims 1 to 10,

in which the at least one discrete circuit element (SE) disposed on the surface of the multi-layer substrate forms at least a part of a high-frequency circuit, an adjustment circuit, an impedance converter, an antenna circuit, a diode circuit, a high-pass filter, a low-pass filter, a band-pass filter, a band elimination filter, a power amplifier, a diplexer, a duplexer, a coupler, a directional coupler, a memory element, a balun or a mixer.

12. Component according to at least one of Claims 1 to 11,

in which the at least one discrete circuit element (SE) disposed on the surface of the multi-layer substrate forms at least a part of a high-frequency circuit, a duplexer or a diplexer, wherein said circuit element connects the at least one chip component (CB) with an antenna.

13. Component according to at least one of Claims 1 to 12,

in which the at least one circuit element integrated in the multi-layer substrate (MS) forms at least a part of a high-frequent circuit, an adjustment circuit, an antenna circuit, a diode circuit, a high-pass filter, a low-pass filter, a band-pass filter, a band elimination filter, a power amplifier, a diplexer, a duplexer, a coupler, a directional coupler, a memory element, a balun or a mixer.

14. Component according to Claim 13,

in which at least a part of an adjustment circuit integrated in the multi-layer substrate is formed as one or more strip conductors on the upper side of the multi-layer substrate for later fine-tuning.

15. Component according to at least one of Claims 1 to 14,

in which the multi-layer substrate (MS) comprises a plurality of adjustment circuits.

16. Component according to at least one of Claims 1 to 15,

in which the multi-layer substrate (MS) contains ceramic layers.

17. Component according to at least one of Claims 1 to 16,

in which the multi-layer substrate (MS) contains layers of silicone or silicone oxide.

18. Component according to at least one of Claims 1 to 17,

in which the multi-layer substrate (MS) contains layers of an organic material, such as plastic or laminate.

19. Component according to at least one of Claims 1 to 18,

in which at least one input and/or at least one output of the at least one chip component (CB) is used to conduct an asymmetrical signal.

20. Component according to at least one of Claims 1 to 19,

in which the at least one input and/or the at least one output of the at least one chip component (CB) is used to conduct a symmetrical signal.

21. Component according to at least one of Claims 1 to 20,

in which the connections to ground of the at least one chip component (CB) are connected with an adjustment circuit at least partially integrated in the multi-layer substrate against the reference ground of the overall component, wherein said adjustment circuit comprises at least one element selected from among a coil, a capacitor or a line segment.

22. Component according to at least one of Claims 1 to 21,

in which both the at least one chip component (CB) and the at least one discrete circuit element (SE) disposed on the upper side of the multi-layer substrate (MS) constitute SMD elements (surface mounted design elements).

23. Component according to at least one of Claims 1 to 22,

in which the at least one chip component (CB) comprises a housing (GE) having external contacts (AE).

24. Component according to at least one of Claims 1 to 23,

in which the at least one chip component (CB) is connected with the multi-layer substrate (MS) by means of wire bonding.

25. Component according to at least one of Claims 1 to 23,

in which the at least one chip component (CB) is connected with the multi-layer substrate (MS) by means of flip-chip technology.

26. Method for the production of the component according to at least one of Claims 23 to 25,

comprising the following steps:

- installation of a chip into a housing (GE),
- mounting of the housing onto a multi-layer substrate (MS).

27. Method according to Claim 26,

wherein the at least one discrete circuit element (SE) is mounted on the upper side of the multi-layer substrate (MS).

28. Method according to Claim 27,

wherein the at least one chip component (CB) and the at least one circuit element (SE) are attached to the upper side of the multi-layer substrate (MS) in the same fashion.

29. Method according to at least one of Claims 26 to 28,

wherein the at least one chip component (CB) disposed on the upper side of the multi-layer substrate and/or the at least one circuit element (SE) is mechanically stabilized with a casting compound.

Abstract

ELECTRONIC COMPONENT

An electronic component includes a multi-layer substrate having an upper side and under side, and at least one integrated impedance converter. The electronic component also includes at least one chip component having external contacts. The at least one chip component is disposed on the upper side of the multi-layer substrate, and is electrically connected to the at least one integrated impedance converter.